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A multiport isolated DC-DC converter

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***Abstract*—This paper presents a multi-port isolated DC-DC converter for DC applications. A three-port structure is presented, characterized with full bidirectional power flow and simple control. Galvanic isolation is achieved by means of a multi-winding medium frequency transformer which is a part of a resonant LLC converter. To provide controllable power exchange with external DC ports, two out of three ports are equipped with additional bidirectional buck/boost stages. They serve to provide active power flow control, while the inner resonant stage provides galvanic isolation, operates in the open-loop and adapts its mode of operation based on the actual power flow. Both switched mode and rea-time hardware-in-the-loop simulations, with control algorithm deployed on the digital signal processor, are used to verify and demonstrate various operational modes.**

I. Introduction

Most of the newly installed energy sources (e.g. PV) or storage technologies (e.g. batteries) are DC by nature, resulting in an increased interest in the development of small or large scale DC grids. Flexibility and simplicity of interfacing power electronics as well as suitable protection technologies are the key to enable new grid architectures. Considering energy production, consumption and storage, multi-port power electronic converters are viable solution to bring together all three aspects and meet demands of micro-grids, while being fully flexible for the integration of different technologies on each side.

So far, only a few investigations related to high power multi-port converters have been reported. The work of [1] deals with converters based on interconnection through a common DC bus. Despite some advantages due to the simplicity of the control, the voltage range is limited and defined by choice of the bus voltage. This limitation can be overcome by means of electromagnetic coupling through medium or high frequency transformers. In [2],[3] and [4] authors have presented solutions derived from the Dual Active Bridge (DAB) or Dual Half Bridge (DHB) with inclusion of additional ports. Limited soft switching operating range of DAB, resulted in considerations towards the resonant converters thanks to their advantages in reduced switching losses. A multi-port LLC converter has been presented in [5] and consists of a three winding medium frequency transformer (MFT) with distributed resonant capacitors tuned to multiple leakage inductors, in order to create resonant tank. The authors have presented configuration where one port act as a source, while two other ports are acting as sink (load). Experiments from a low power setup (300W), demonstrate good load regulation but gave no consideration to different operating modes. On the other hand, work of [6] shows a similar topology where two ports are configured as sources and are equipped with resonant capacitors, while the third port has only a rectifier as it is behaving as the load. Authors have demonstrated controllable power flow and load sharing between sources, using phase shift control. While, several works have been dealing already with LLC or multi-port converters, the focus has been mainly on a low power rated converters and unidirectional power flow.

This paper is an extension of the previous work [7] and it presents a novel multi-port topology and its operation in section II. Design considerations and sizing of main components are presented in section III, while the control scheme is provided in section IV. PLECS simulations as well as hardware-in-the-Loop simulations, with control algorithm deployed on the digital signal processor (DSP) are given in section V. A summary and conclusion are provided in section VI.

II. Topology and Operating Modes

The topology considered in this paper is based on a three winding medium frequency transformer as shown in Fig. 1. It is fully bidirectional, even with one of the three ports deactivated. The converter basic stage is composed of a multi-port LLC resonant circuit equipped with two additional buck/boost stages. The ports may have different power ratings ($P_1 \neq P_2 \neq P_3$) and arbitrary output voltages ($V_{DC_1} \neq V_{DC_2} \neq V_{DC_3}$).

A. Multiport LLC Resonant Stage

The inner part is made by a three winding MFT with turn ratio n_i according to the desired output voltages and equipped with three half bridges. In order to achieve high efficiency, a resonant LLC topology is used and operated in the open-loop mode below resonant frequency [8]. Since the full bi-directionality of the converter implies certain symmetry requirements, the resonant tank is not located on a single port, like in [5], but is split between all three ports. Each resonant tank is composed of a capacitor C_i and an inductor L_i which is the combination of the stray inductor of the MFT and, if needed, an additional inductor. The design of the resonant tank requires proper sizing of all distributed L_i and C_i in a way that guaranties soft switching conditions for any operating point within the power specifications. The resonant part is intended to be operated as a DC transformer without any complex control scheme. It is only controlled by activating or deactivating PWM on $S_{1,2,3}$, depending on the power flow direction. Only the ports that are providing power

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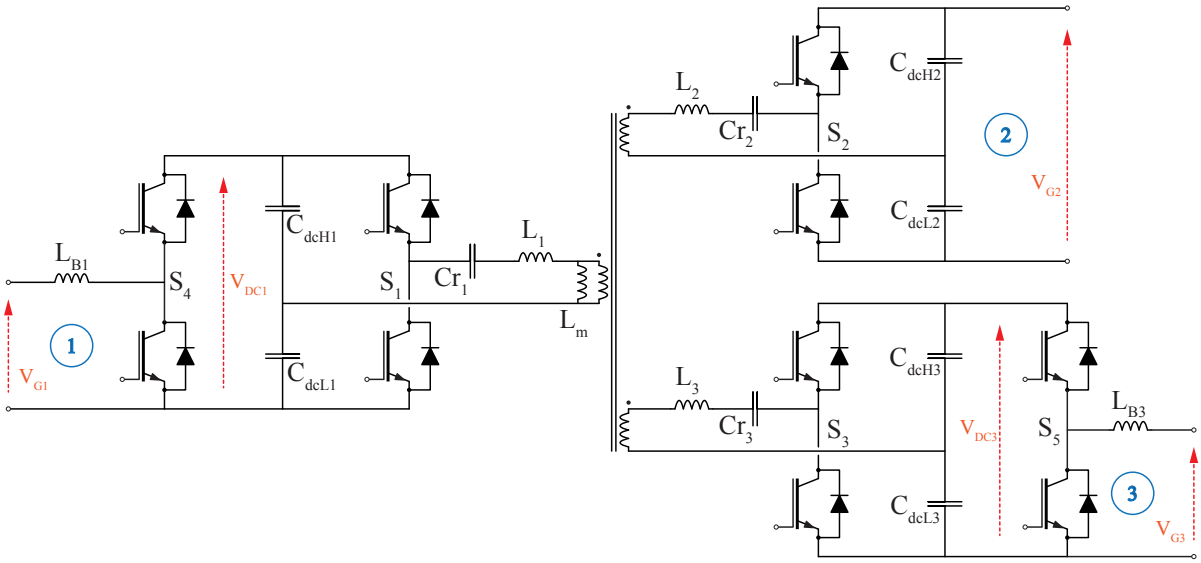

Fig. 1. Topology of a Multiport Isolated DC-DC Converter

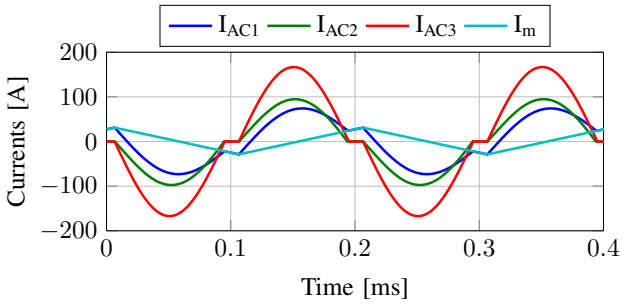

Fig. 2. Source port: 1 ($P_1 = 90kW$); Sink ports: 2 ($P_2 = -50kW$) and 3 ($P_3 = -40kW$)

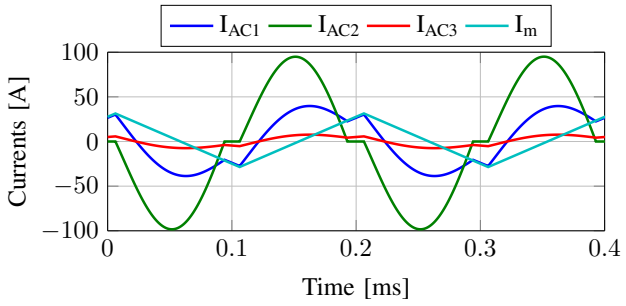

Fig. 3. Source ports: 1 ($P_1 = 50kW$) and 3 ($P_3 = 10kW$); Sink port: 2 ($P_2 = -60kW$)

are actively switched. Load ports are turned off and their freewheeling diodes are used as passive rectifiers (voltage doubler configuration as shown in Fig. 1). When a port is active, its high and low side switches are operated with opposite polarity at a fixed frequency f_{sw} and a constant duty cycle of approximately 50% (considering dead-time). Typical current waveforms in such a structure are shown in Fig. 2 and Fig. 3.

B. Buck/Boost Stages

Since no active control is applied on the inner resonant stage, the power flow must be regulated by two additional stages (S_4 and S_5) on the ports 1 and 3. These stages are based on a bidirectional buck/boost converter and thus can be operated either as boost or as buck depending on the actual mode of operation, as it will be discussed shortly.

C. Operating Modes

There are several operating modes of this converter that influence the overall control scheme, as summarized in Table I. The resonant stage modes, related to switching cells S_1, S_2 and S_3, simply describe if the respective switching cells are active (PWM on) or passive (PWM off). However, the operation of S_4 and S_5 define if the stage is used as boost or buck converter. In this paper, ports 1 and 2 are the main ports rated for the full power of the converter and in charge of the power flow. Bidirectional operation implies that power flow from the port 1 to the port 2 (modes A1, B1 and C1) or vice versa (modes A2, B2 and C2). In both cases, the voltage on port 2 is directly controlled through port 1 by the buck/boost stage S_4. Port 3 is considered as an additional port that can source (mode B1 and B2) or sink (mode A1 and A2) power with reduced ratings, regardless of the power direction between the ports 1 and 2. Its buck/boost stage S_5, regulates the current I_{b3}, compensating

for voltage variations due to cross-coupling with ports 1 and 2. In the modes C1 and C2, no energy is exchanged with the port 3 and S_5 is deactivated.

Previous description assumes that multiport converter controls its voltage on port 2, however in case of presence of additional converter, (e.g. AC grid connected inverter), overall role of different ports may change, as it is usually the grid side converter that controls its DC link voltage (e.g. port 2 voltage).

TABLE I
OPERATING MODES

Mode	S_1	S_2	S_3	S_4	S_5
A1	Active	Passive	Passive	Boost	Buck
A2	Passive	Active	Passive	Buck	Buck
B1	Active	Passive	Active	Boost	Boost
B2	Passive	Active	Active	Buck	Boost
C1	Active	Passive	Passive	Boost	Off
C2	Passive	Active	Passive	Buck	Off

III. DESIGN METHODOLOGY

For this case study, power and voltage ratings are chosen somewhat arbitrarily and are summarized in Table II.

TABLE II
POWER AND VOLTAGE RATINGS USED FOR THE CASE STUDY

Port	P_i	V_{DC_i}	V_{G_i}
1	125 kW	3600 V	3000 V
2	125 kW	1500 V	1500 V
3	25 kW	750 V	400 V

A. LLC Tank Design

The design of the resonant part is based on a methodology presented in [7]. The aim is to determine the resonant parameters in such a way that ensures the ZVS of the primary switches (active port), soft commutation of rectifier diodes (passive port) and minimize the amount of circulating energy (conduction losses). For a given ratio f_n, of the switching and the resonant frequency and for a given operating point represented by an AC load R_{AC_i}, the maximum value of L_{r_i} required to stay in the inductive region is given by:

$$L_{max_i} = \frac{f_n R_{AC_i} \pi^2}{8\sqrt{2}\omega_0} \tag{1}$$

The quality factor Q_{opt_i} is defined as the ratio between the load and the tank impedance, under the maximum load conditions, for which the tank RMS current is the smallest. For the operating point given by R_{AC_i}, the resonant inductor which provides the optimal quality factor is defined, according to [9] and [10], as:

$$L_{opt_i} = \frac{R_{AC_i}^2}{\omega_0^2 L_{m_i}} \tag{2}$$

$$Q_{opt_i} = \frac{R_{AC_i}}{\omega_0 L_{m_i}} \tag{3}$$

We can then obtain the optimal Q factor for each port. The distributed resonant inductors are calculated from the equations linking the three power quality factors to the three resonant inductors:

$$L_i \leq Q_{opt_i} R_{AC_i} - \left(\frac{1}{(n_i/n_j)^2 L_j} + \frac{1}{(n_i/n_k)^2 L_k} \right)^{-1} \tag{4}$$

$$C_i = \frac{1}{L_i (2\pi f_{res})^2}; i \neq j \neq k \tag{5}$$

Resulting parameters for the L_i and the C_i are shown in Table III.

In order to benefit from the ZVS, the magnetizing inductor has to be sized accordingly. Its value will define the turn-off current of the active ports and thus turn-off switching losses. Since this turn-off current corresponds to the negative turn-on current of the free-wheeling diode of the complementary switch, its value cannot be selected too low. To preserve ZVS, the resonant tank current should not change polarity within the dead-time. The duration of diode conduction can be approximated by division of the turn-off current by the slope of the resonant tank current at this point. To maintain ZVS within the dead-time T_{dt}, L_m must satisfy:

$$I_{off_{min}} \approx T_{dt} I_{DC_n} \frac{\pi}{2} \tag{6}$$

$$L_{m_i} \leq \frac{V_{DC_i} T_{sw}}{8 I_{off_{min}}} \tag{7}$$

Considering that the quality factor Q is linked to the magnetizing inductor through (3), it has to be chosen such to keep the optimal L_{opt}, smaller than L_{max}:

$$L_{m_i} \geq \frac{R_{AC_i} 8\sqrt{2}}{\omega_0 f_n \pi^2} \tag{8}$$

The magnetizing inductors seen from each port, L_{m_i} must fulfill the condition of (7) and (8) for all three ports:

$$L_{m_1} = L_m \qquad L_{m_2} = L_m \frac{n_2^2}{n_1^2} \qquad L_{m_3} = L_m \frac{n_3^2}{n_1^2} \tag{9}$$

Resulting parameters of the distributed resonant tank, for the ratings used in this paper, are summarized in Table III.

B. DC Link Capacitors Sizing

DC link capacitors are sized according to voltage ripple specifications and resulting values are shown in Table IV.

$$C_{DC_i} = \frac{V_{DC_i} T_{sw}}{2 R_{dc} \Delta V_i} \tag{10}$$

$$C_{dcH_i} = C_{dcL_i} = 2 C_{DC_i} \tag{11}$$

Since DC capacitors are in series with the resonant tank, resonant capacitors are adjusted to match the value calculated in (5).

$$C_{r_i} = \frac{C_i 4 C_{DC_i}}{4 C_{DC_i} - C_i} \tag{12}$$

TABLE III
DISTRIBUTED RESONANT TANK PARAMETERS

L_m	10.0 mH	$f_{sw_{llc}}$	5 kHz
L_1	13.7 μH	C_1	66.6 μF
L_2	2.6 μH	C_2	354.1 μF
L_3	29.8 μH	C_3	30.7 μF

TABLE IV
DC LINK CAPACITORS FOR EACH PORT

$Port_i$	$\Delta V_i/V_{dc_i}$	ΔV_i	C_{DC_i}	C_{r_i}
1	0.01	36 V	96.5 μF	80.5μF
2	0.01	15 V	555.6 μF	421.2μF
3	0.01	7.5 V	444.5 μF	31.23μF

C. Buck/Boost Stage Design

The switching frequencies for the two buck/boost stages are chosen in such a way that switching frequency of the port 1 is lower than the LLC switching frequency, while the switching frequency of the port 3 is higher. It should be noted that present values are not result of any optimization, since actual hardware design is not the main scope of this paper. Chosen values are shown in Table V. The buck/boost inductors are sized according to the ripple specifications.

$$L_{B_i} = \frac{V_{G_i} T_{sw_{boosti}}}{2\Delta I_{b_i}} \tag{13}$$

TABLE V
BUCK/BOOST STAGES PARAMETERS

F_{B_1}	2.5 kHz	$\Delta Ib1$	4 A	L_{B_1}	40 mH
F_{B_3}	10 kHz	$\Delta Ib3$	4 A	L_{B_3}	5 mH

IV. CONTROL SYSTEM DESIGN

Simplified control scheme is presented here, considering different ratings for the ports. The output voltage of the port 2 is regulated from the port 1 buck/boost S_4 stage while the power through port 3 is locally regulated by its own buck/boost stage S_5. In this way a large degree of freedom exists for integration of different energy storage technologies on port 3.

A. Plant model

Considering that the resonant stage is operated in an open-loop with a fixed switching frequency, its DC transfer function (gain) is considered constant and close to unity. For that reason it is neglected in the analysis and the DC link capacitors can be considered in parallel, taking into account the turn ratio of the transformer. Thus the circuit can be modeled as shown in Fig. 4. The voltage of the port 2, proportional to the voltage $V'_{C_{DC}}$ on C'_{DC} (14), has to be regulated and the control input is the duty-cycle D_1 of the buck/boost stage S_4. The perturbations to this circuit are the voltage on the buck/boost S_4 input V_{G1} and the currents in ports 2 and 3, I'_2 (15) and I'_3 (16), respectively (all referred to port 1 side). The buck/boost stage S_5 current (I_{b3}) has to be regulated and the control input is its duty-cycle D_3. The perturbation to this part is the voltage on C_{DC}

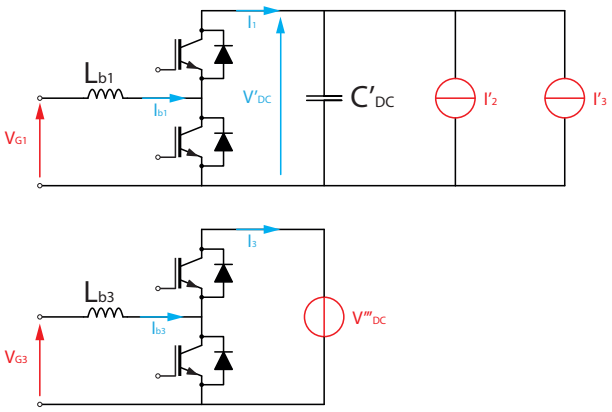

Fig. 4. Simplified model of the converter assuming unity transfer function of the resonant stage

referred to the third winding. The average model of two sub-circuits from Fig. 4 is represented in Fig. 5, where $G_{I_1}(s)$ (18), $G_{I_3}(s)$ (20) are the transfer functions of the boost inductors L_{B_1}, L_{B_3} and $G_{Uc}(s)$ (19) is the transfer function of the combined DC capacitors C_{DC}.

$$C'_{DC} = C_{DC_1} + \frac{n_2^2}{n_1^2} C_{DC_2} + \frac{n_3^2}{n_1^2} C_{DC_3} \tag{14}$$

$$I'_2 = \frac{n_2}{n_1} I_2 \tag{15}$$

$$I'_3 = \frac{n_3}{n_1} I_3 \tag{16}$$

$$V'''_{DC} = \frac{n_3}{n_1} V'_{DC} \tag{17}$$

$$G_{I_1}(s) = \frac{1/R_{l_1}}{1 + s(L_{b_1}/R_{l_1})} = \frac{K_{I_1}}{1 + sT_{I_1}} \tag{18}$$

$$G_{Uc}(s) = \frac{1}{sC'_{DC}} = \frac{1}{sT_U} \tag{19}$$

$$G_{I_3}(s) = \frac{1/R_{l_3}}{1 + s(L_{b_3}/R_{l_3})} = \frac{K_{I_3}}{1 + sT_{I_3}} \tag{20}$$

B. Control system

Rather simple control approach has been followed and the voltage on the port 2 is regulated through two cascaded PI loops. The inner loop controls the inductor current I_{B_1} with the PI regulator G_{RI_1} while the outer loop controls the voltage V_{DC_2} with the PI regulator G_{RU}. The current in the port 3 is regulated with a single PI loop and the regulator G_{RI_3}. Please note that in case of a connection of energy storage (e.g. battery, ultra-capacitors) there would be a need for outer loop for the purpose of the energy management. This is however not the scope of this paper and the used control structure is presented in Fig. 6, with the parameters of the regulators provided in the Table VI. These values are obtained according to description provided in the Appendix.

The control structure shown in Fig. 6 does not include all implementation details associated with the changes of the modes of operation. To avoid large inrush currents during the

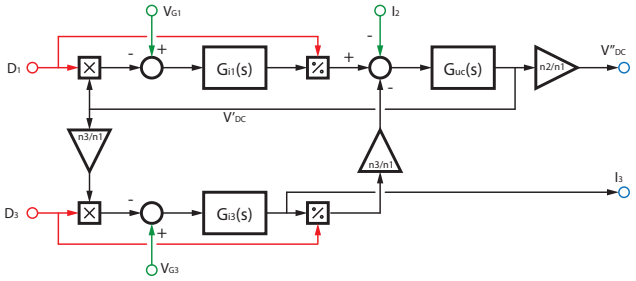

Fig. 5. Average model of the circuit from Fig. 4

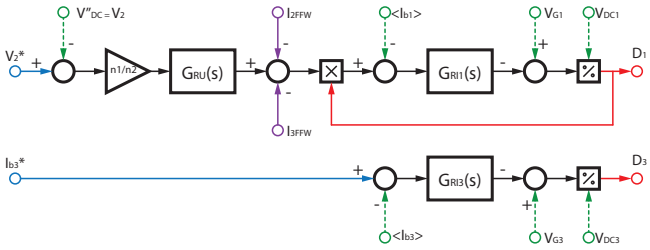

Fig. 6. Control structure used in conjunction with the model from Fig. 5

TABLE VI
PI REGULATOR'S PARAMETERS

$T_{n_{I1}}$	0.8	$T_{i_{I1}}$	0.012
$T_{n_{uc}}$	0.0032	$T_{i_{uc}}$	0.0241
$T_{n_{I3}}$	0.1	$T_{i_{I3}}$	0.018

startup of S_1, S_2 or S_3, the duty cycle is ramp-up to final 50%. During this transition sequence, the ZVS is not necessarily achieved.

V. Simulation Results

To verify design of the distributed resonant tank and the performance of the control scheme in the different modes of operation, different simulations have been performed. The closed-loop switched model has been implemented in PLECS as well as on the real-time power electronics hardware-in-the-loop (HIL) simulator controlled with digital signal processor (DSP).

A. PLECS Simulations

Simulation results with several mode transitions are shown in Fig. 7 and 8. The unfiltered DC voltages of the resonant stage are shown in the upper plots in per unit values, while the RMS and average values of relevant currents, respectively, are shown in the bottom plots. Detailed description of the simulation scenarios is provided in the captions of Fig. 7 and 8. As it can be seen, the output voltage V_{DC_2} has been effectively regulated to its rated value, in all modes of operation.

B. HIL Simulations

As a second step, the complete converter has been modeled and deployed on the Typhoon HIL 400 real-time power

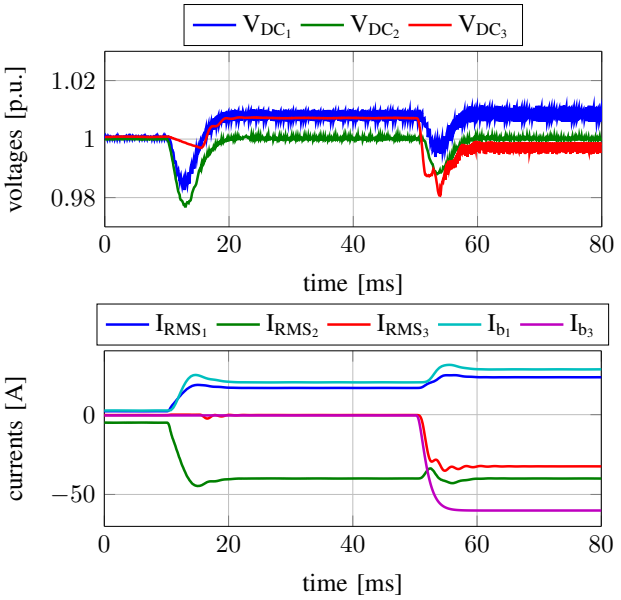

Fig. 7. PLECS simulations: At t=10ms, the load on the port 2 is increased from 0 to -40A. The current in the boost S_4 tracks this current step resulting in an increase of V_{DC_1}. After the transient, the voltage V_{DC_2} returns to its reference (1 p.u.). At t=50ms, the load on the port 3 is increased from 0 to -60A resulting in a decrease of V_{DC_3}. After the transient, I_{RMS_2} remains the same and I_{RMS_1} is slightly increased by its contribution in I_{RMS_3}. V_{DC_2} is regulated back to 1 [p.u.]

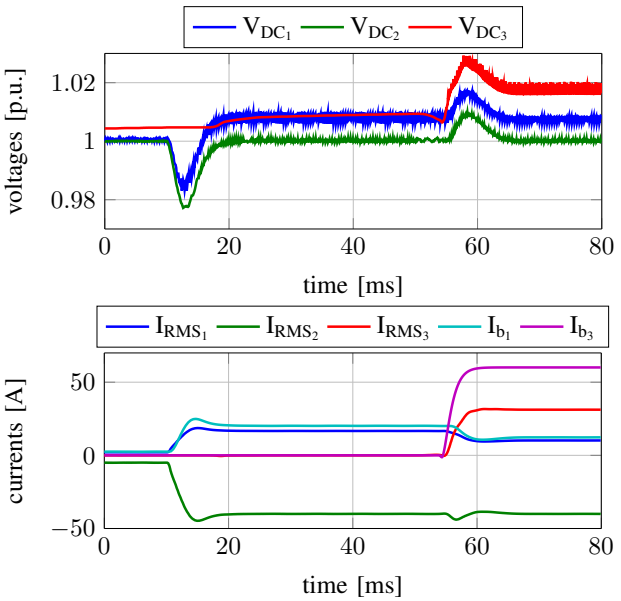

Fig. 8. PLECS simulations: At t=10ms, the load on the port 2 is increased from 0 to -40A. I_{B_1} follows this current step resulting in an increase of V_{DC_1}. Since there is no power exchange through the port 3, S_5 is deactivated and V_{DC_3} is following V_{DC_1}. At t=50ms, S_3 is turned on and starts with a modulation ramp. At t=55ms the ramp is finished and the buck/boost stage S_5 of port 3 starts to regulate the current I_{b_3} to 60A.

electronics simulator, while the control algorithm has been

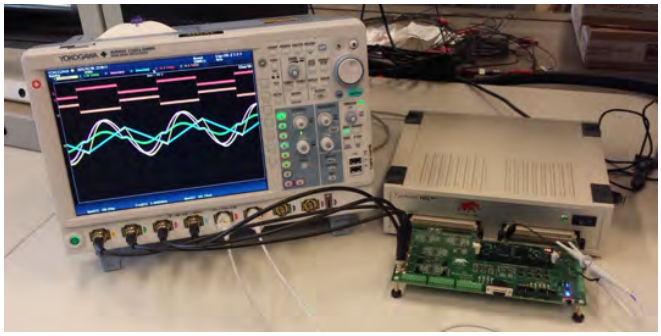

Fig. 9. HIL test setup with TI C2000 DSP

implemented on the TI TMS320F28335 DSP. This allows to carry out the simulations of numerous test cases and verify performances of the digital controller in the real-time. The complete test setup is shown in Fig. 9 (actual resonant current waveforms observed during testing are visible on the scope), while the captions of Fig. 10 and 11 provide description of the modes of the operation. Change of loading conditions on the port 3 has been tested and closed loop response of the control algorithm responsible for the main ports has been successfully verified.

VI. Conclusions

The topology of a bidirectional multiport resonant DC-DC converter has been presented in this paper. It is based on the combination of an open-loop operated multiport resonant converter with distributed resonant tank, and additional closed-loop operated boost/buck stages on two ports. The operating modes of the converter have been described and suitable control scheme is presented. The inner resonant stage operates as DC transformer, and its main function is to provide galvanic isolation between different ports. Auxiliary third port has reduced ratings and is intended for connection of electrical energy storage elements, as support for the main ports.

Simulation results demonstrate operating principles, while further verification has been performed with digital controller deployed on the DSP and tested in the real-time with hardware-in-the-loop simulator. Topology, of the presented multiport converter, allow for further extensions for the higher operating voltages. Several converter stages from Fig. 1 can be stacked in input-series (port 1) output-parallel (port 2) fashion, with multiple ports 3 either left floating or tied together. In this way, connection to the higher DC voltages on the port 1 side is possible (insulation requirements for the MFT are naturally increased). This, together with the hardware design is the subject of the ongoing work, and will be reported separately.

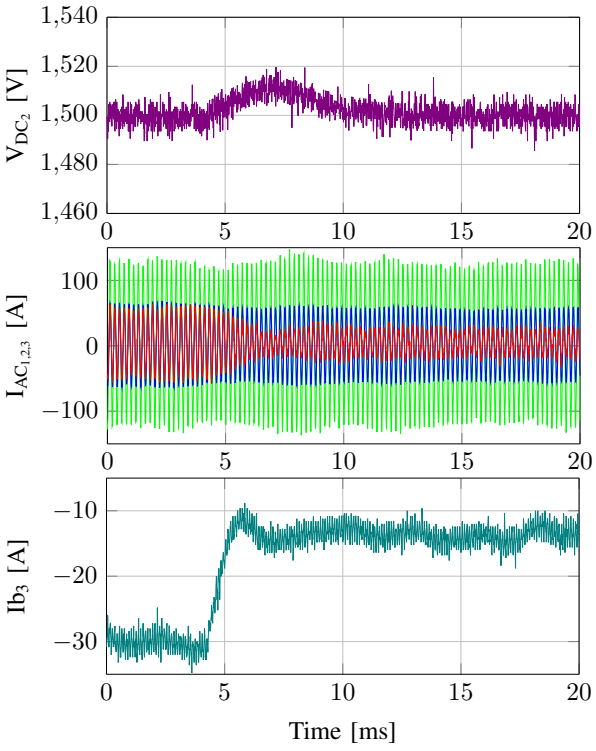

Fig. 10. HIL simulations: At t=4ms, the load on the port 3, I_{b_3} is decreased from -30 to -15 A. In response, the voltage on the port 2 V_{DC_2} is slightly increased, but immediately regulated by buck/boost stage S_4 of the port 1. All three resonant tank currents are shown in the middle plot, from where their envelope values can be observed.

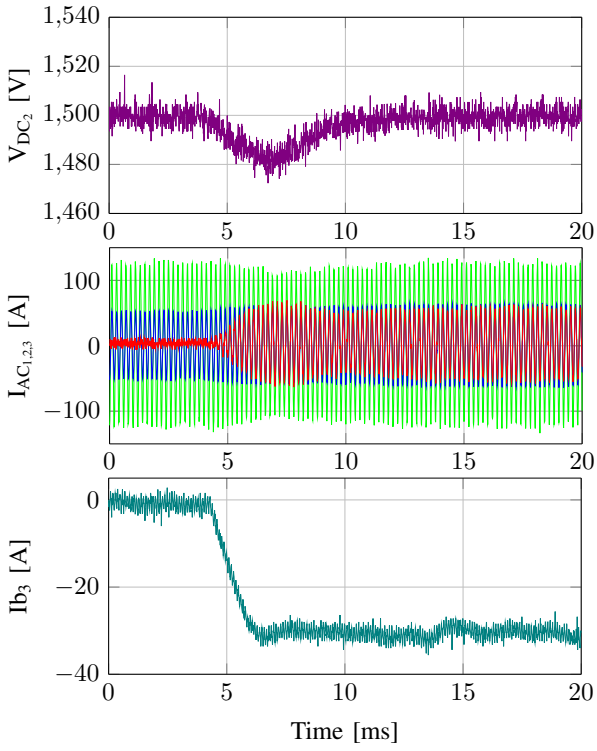

Fig. 11. HIL simulations: At t=4ms, the load on the port 3, I_{b_3} is increased from 0 to -30 A. In response, the voltage on the port 2 V_{DC_2} is slightly decreased, but immediately regulated by the buck/boost stage S_4 of the port 1. All three resonant tank currents are shown in the middle plot, from where their envelope values can be observed.

ACKNOWLEDGEMENT

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APPENDIX

The parameters of the regulators G_{RI_1} and G_{RI_3} are determined according to the principle of the symmetric optimum while the regulator G_{RU} is tuned according to the principle of the magnitude optimum.

$$T_{PE_1} = 0.5T_{sample} + T_{sw_{boost1}} \tag{21}$$
$$T_{n_{I1}} = T_{I_1} \tag{22}$$
$$T_{i_{I1}} = 2K_{I_1}T_{PE_1} \tag{23}$$

$$T_{CL} = 0.5T_{sample} + 2T_{PE_1} \tag{24}$$
$$T_{n_U} = 4T_{CL} \tag{25}$$
$$T_{i_U} = 8T_{CL}^2/T_U \tag{26}$$

$$T_{PE_3} = 0.5T_{sample} + T_{sw_{boost3}} \tag{27}$$
$$T_{n_{I3}} = T_{I_3} \tag{28}$$
$$T_{i_{I3}} = 2K_{I_3}T_{PE_3} \tag{29}$$

Please note that for the simulation studies, the sampling time T_{sample} is equal to the switching period of the resonant stage T_{sw}. Resulting parameters of the regulators are given in Table VI.

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